

Impact of a SADP flow on the design and process for N10/N7 Metal layers

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Abstract

This work addresses the difficulties in creating a manufacturable M2 layer based on an SADP process for N10/N7 and proposes a couple of solutions. For the N10 design, we opted for a line staggering approach in which each line-end ends on a contact. We highlight the challenges to obtain a reasonable process window, both in simulation as on based on exposures on wafer. The main challenges come from a very complex keep mask, consisting of complicated 2D structures which are very challenging for 193i litho. Therefore, we propose a solution in which we perform a traditional LELE process on top of a mandrel layer. Towards N7 we show that a line staggering approach starts to break down and design needs to allow better process window for lithography by having metal lines ending in an aligned fashion. has many challenges and we propose to switch to a line cut approach. A more lithography friendly approach is needed for design where the lines end at aligned points so that the process window can be enhanced.

1. Introduction

Self-aligned double patterning (SADP) is an important patterning technique that is needed for allowing scaling of metal pitch down to the 42nm pitch. In order to achieve successful decomposition, an SADP-compliant design becomes a necessity. Compared to Litho-Etch-Litho-Etch (LELE) double patterning lithography (DPL), spacer defined patterning techniques have clearly advantages with respect to overlay tolerance and line-width roughness (LWR). However the key challenge of SADP or SAQP approaches is how the line ends. This pushes the problem to keep or block masks that are used to terminate lines. This paper evaluates for different metal pitches ranging from 48nm down to 32nm, different metal patterning techniques that can be used and which give the largest process window to be eventually usable in industry

The paper is organized as follows: the next section describes standard cell template that has been used for the rest of the paper. Section 3 describes the different place and route options that can be used for the tight metal layers. As pitches move to 48nm for N10 and 32-28nm for N7 are considered the most viable option for tight pitch Mx layers.

2. Standard cells

For evaluating M2 it is crucial that the right design context is considered and this needs to be done post place and route of a complete design. For this purpose we have designed standard cells for both N10 as well as for N7 technologies with similar templates. The ground rules used for these designs are summarized in the table below:

Layer	N10 Patterning	N10 Pitch	N7 Patterning	N7 Pitch
Vertical M1	SADP	64nm	SADP	42nm
Horizontal M2	SADP	48nm	SAQP	32nm
V1	LELE		LELELE(LE)	
Fin	SADP	36nm	SAQP	24nm

The design of standard cells template was made generic to both N10 and N7 technology nodes. As described in paper [x], we have explored different standard cell styles, and evaluated the pros and cons of each of them. Given SADP/SAQP assumptions on the metal layers, a strictly unidirectional routing has been used to all metal layers. For the place and route experiments we have pursued the style with M1 vertical to the gate at the gate pitch. This template also forms a gear ratio of $\frac{3}{4}$ between the fins and the metal allowing building 8 active fins in the 9 track cell. A standard cell library consisting of about 50 cells with 9 metal tracks has been developed. A few snapshots of these standard cells are illustrated in Figure 1. More information about these templates can be found in [1].

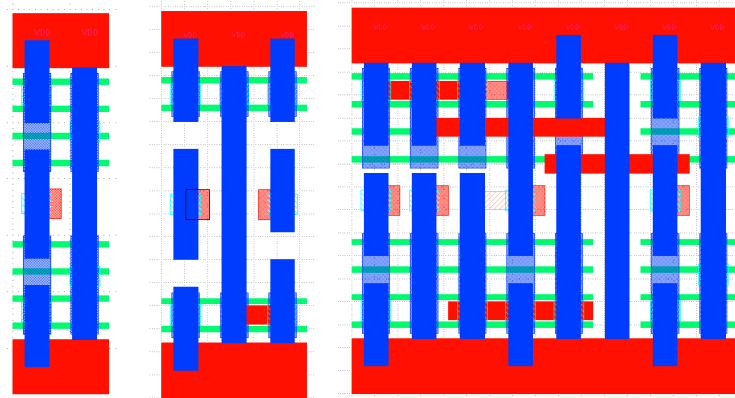


Figure 1: 1D Standard Cell with Vertical M1 (blue) and Horizontal M2 (red)

3. Place and route options for Metal

In order to take benefit of an SADP/SAQP flow, N10/N7 Mx layers need to be kept strictly 1D. For initial trials we performed place and route with 2D freedom to the router, while remaining SADP and keep mask compliant in terms of decomposition. With the 2D freedom for the router, there were very few places in the die where the router used the 2D freedom to land on vias. However given the limited use of the 2D constructs and no area overhead of restricting to 1D routing, we constrained the router to perform strictly 1D routing.

Within the constraint of 1D routing, place and route can be done with two styles: i) line and cut or ii) line staggering, both with strict 1D routing. This is illustrated in the figure below. The first style is called line staggering, this is the style where the line ends where the via makes the contact with the metal above or below (shown in the right side of **Figure 2**). The second scheme is known as the line and cut scheme. This is the scheme where the line is extended to the edge of so that cuts (or line ends) are aligned as much as possible. This is illustrated in the left side of the **Figure 2** below.

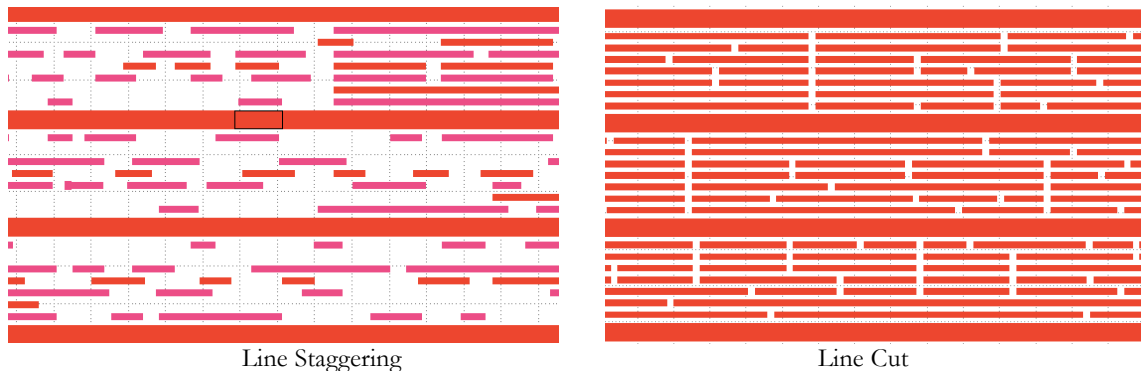


Figure 2: Place and route techniques

The line staggering approach can be decomposed with keep or block mask fashion. The number of keep-masks needed depend on the pitch and the process window. However given that the line cut approach has most of the die covered with metal, keep-mask based printing would not work and a block based approach makes more sense to follow. **Figure 3** shows the decomposition of the intent metal to one keep mask or two keep masks. The coloring for the two keep mask is relatively simple where the color is alternated between odd and even lines. The multiple keep solution works provided there is no coloring conflict within a single row. At tight metal pitches (N7), as the tip to tip scales down this approach also break down and would require a more complex coloring on the keep mask based approach.

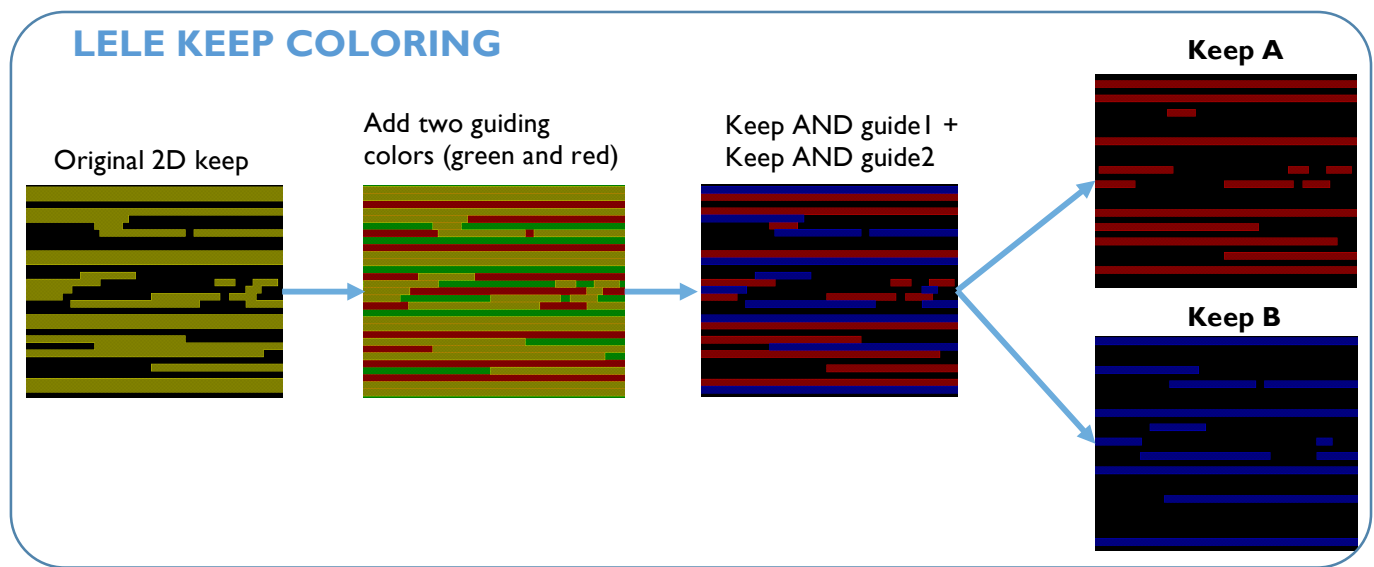
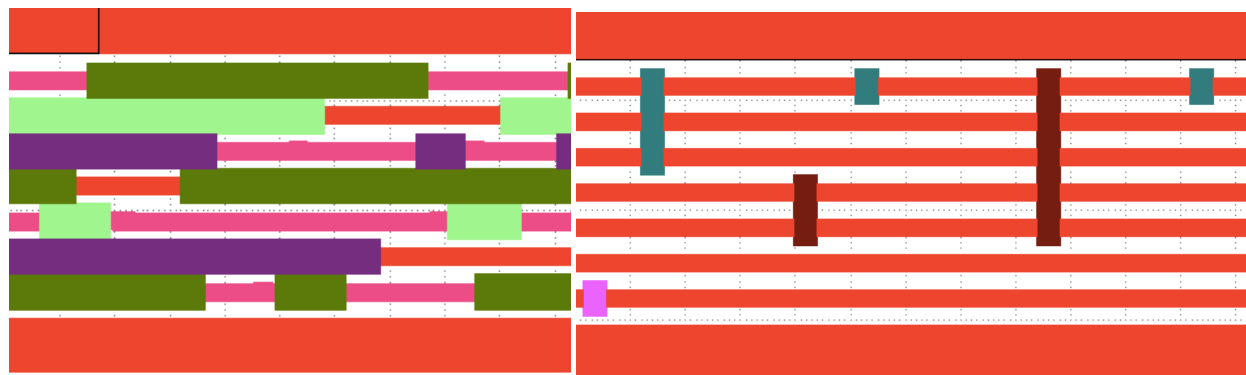


Figure 3: Keep mask coloring

The alternative method of coloring is by the block mask based approach. **Figure 4** shows the decomposition options for block masks for both the design solutions (line cut and line staggering). It can be seen from the figure that the coloring for the line staggering scheme requires the blocks to be stitched at tight pitches. Also when the pitch for the metal is reduced further down to 28nm, the pitch of the block mask will also decrease, therefore this approach is more sensitive to metal pitch. However in case of the line cut, the coloring of the block is coupled to the metal pitch a bit more loosely. For metal pitch of 32nm, the line cut version requires 2 colors (with limited violations that can be fixed), whereas the line staggering requires 3 colors in the block. For a tighter pitch of 28nm, the line cut requires 3 colors whereas the line staggering will require 4 colors.



(a) Block mask decomposition for line staggering approach (b) Block mask decomposition for line cut approach

Figure 4: Block mask coloring

Using the line cut approach increases the average wire length of each net by about 30% on average. This increase translates to increased capacitance in the wires and therefore due to increased power also in the design. However critical paths of the design are not affected much and has no/limited impact in terms of timing of the design. However the line cut has the overwhelming advantage in terms of the block mask requirement. In a metal pitch of 32nm (N7), the line cut approach needs 2 block masks (with limited hotspots). However the line staggering needs 3 block masks at a metal pitch of 32nm. At N10 like dimensions (48nm pitch), the line staggering approach can possibly be used with one or two block or keep masks. The different options for this are further explored in the following sections. Furthermore the block

masks need to be stitched in case of the line staggering scheme to ensure no metal is filled. The other key advantage of the line cut approach is the average metal density in the design is 50% (assuming the metal width is 50% of the pitch). However there is no difference in terms of area between the two options. Table below also summarizes the differences between the two techniques of routing for the block mask scheme.

Line Staggering	Line Cut
Equal Area	Equal Area
Reduced wire length	Increased wire length ~30%
Block mask stitching needed	Simple block mask scheme
Metal density design dependent	Near perfect uniform metal density
For pitch 28nm, 4 block masks needed	For pitch 28nm, 3 block masks needed
For pitch 32nm, 3 block masks needed	For pitch 32nm, 2 block masks needed
Lower capacitance in the BEOL	Increased capacitance (increased power)

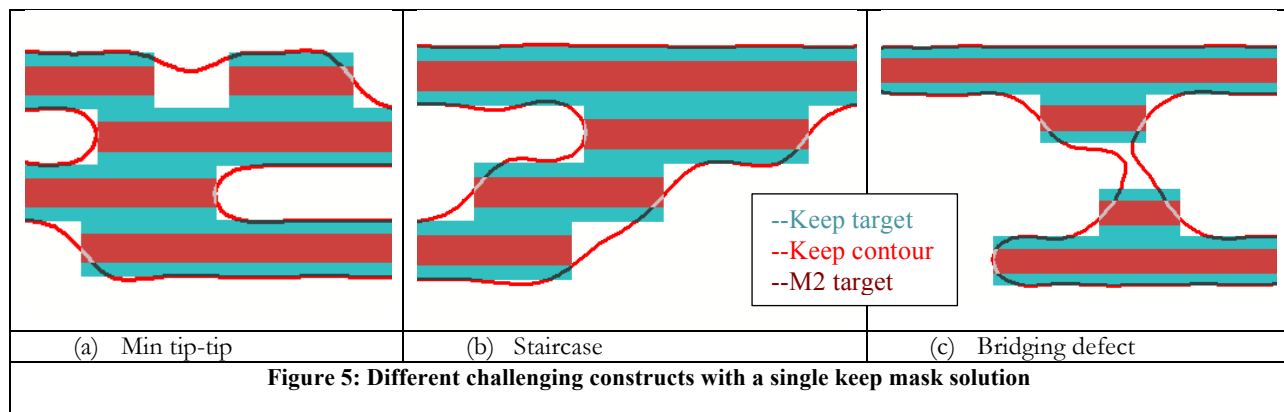
4. N10 Metal 48nm pitch: exposure on wafer

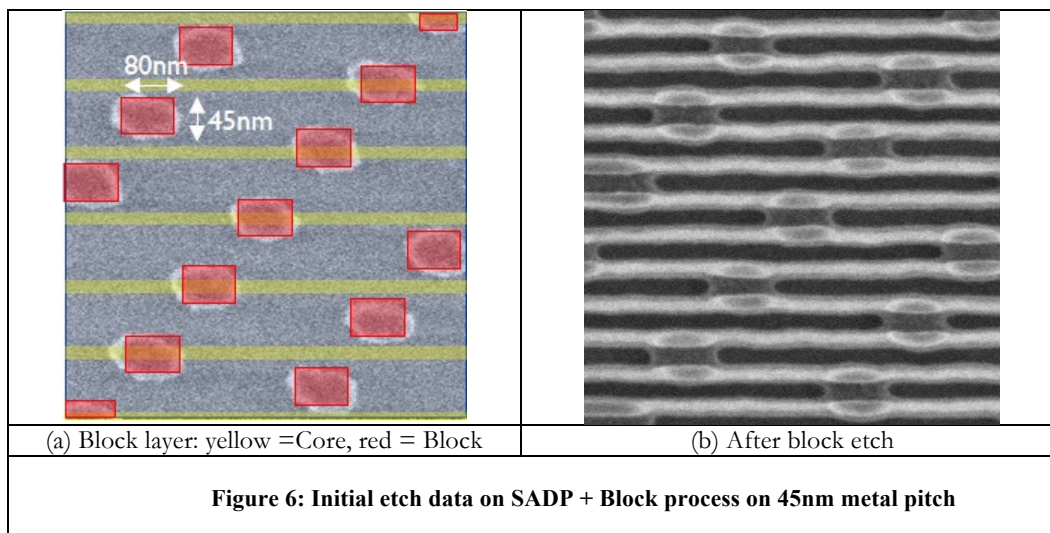
In this section we will describe the patterning challenges and propose a solution for an N10 M2 layer. Since the line staggering approach has the advantage of being compatible with an LELE approach and has the added benefit of lower capacitance, we assumed line staggering as our front-up approach for our N10 design.

After place and route of the design we decomposed the final metal into a core and a keep layer. At this point we started our computational work to assess the printability of the design. For both the Core as the keep layer source-mask-optimization (SMO) was performed. Following this, we calibrated 2 OPC models and tuned the OPC recipes.

As could be expected the core layer did not show many problems, as it is mostly a 1D grating defining the metal CD. The OPC script was optimized with a tight spec on the CD, while the line ends were less strictly controlled. The reason is that the line ends of the final metal are define by the Keep layer.

Problems did start to appear in the keep layer. Some problems could easily be traced back to P&R settings. A typical example is the min tip-to-tip distance. As can be seen in **Figure 5 (a)** the keep cannot cut two metal lines below a certain value. In our case the min tip-to-tip distance needed to be ~80nm in order to resolve this with the keep layer. This rule has a strong impact on chip area and may need to be unacceptably high in order to have a stable process. A second type of defect we found are related to “staircase” configurations [see **Figure 5 (b)**]: in these positions the contours are all diagonal, which will lead to sharp corners on the final metal line ends. These can be quite severe, but we have initial data on an SADP+Block process that shows that those sharp line ends are not transferred during etch (see **Figure 6**). Apart from those, other defects (mainly bridging) were appearing due to some challenging 2D configurations [see **Figure 5(c)**]. Even by using very aggressive OPC, they were proving to be impossible to print with some process window. Even more problematic was the fact that it was not possible to relate those configurations back to the rules imposed to the P&R giving us very little control on the design side to try to improve the process window. In terms of places and route the restrictions needed for enabling these constructs (staircase, min tip-tip and extension from opposite sides) can be imposed, however these cause immediate non-acceptable increase in area of the chip and therefore were not considered.





To verify our simulations we exposed a focus-energy-matrix (FEM) wafer and compared the resist to the target design (see **Figure 7**) and the simulated contour (**Figure 8**)

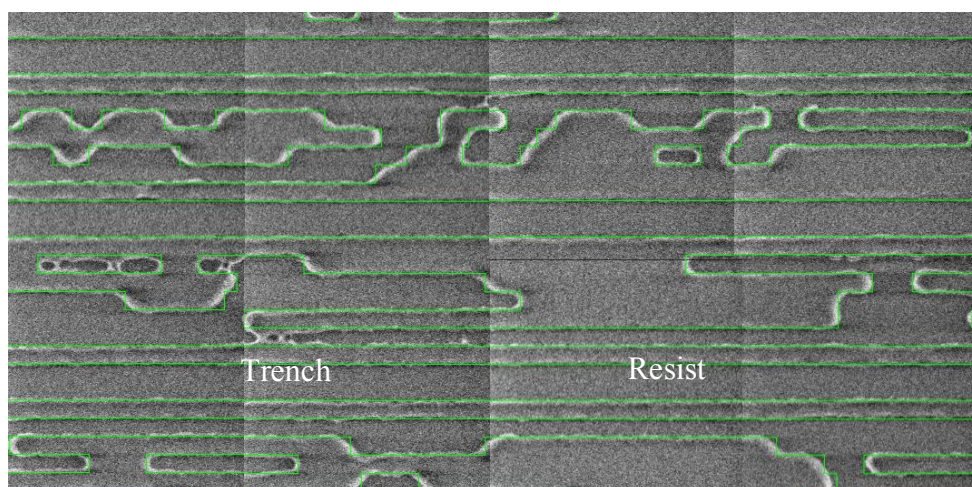


Figure 7: Target design of the keep layer overlapped with SEM images

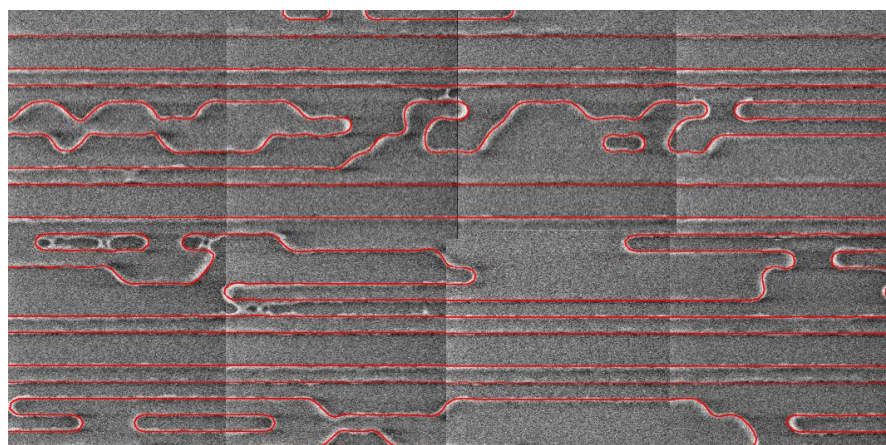


Figure 8: NC simulation contour overlapped with SEM images

It became clear that a good compromise between patternability and chip area was difficult to achieve. Therefore we proposed to split the keep layer and use a spacer assisted LELE approach for this layer. The decomposition itself is easy because all the M2 tracks are on the multiple of the 48nm pitch. Therefore it is sufficient to create a uniform grating of 2 color 96nm pitch lines shifted by $\frac{1}{2}$ pitch and then applying a simple “AND” Boolean operation with original keep (Figure 3).

In Figure 10 we show the difference between the single keep and the LELE-keep approach. The main conclusion is that the final metal has higher pattern fidelity, line ends are better controlled and a larger process window is obtained. Importantly the min tip to tip can be reduced to ~50nm.

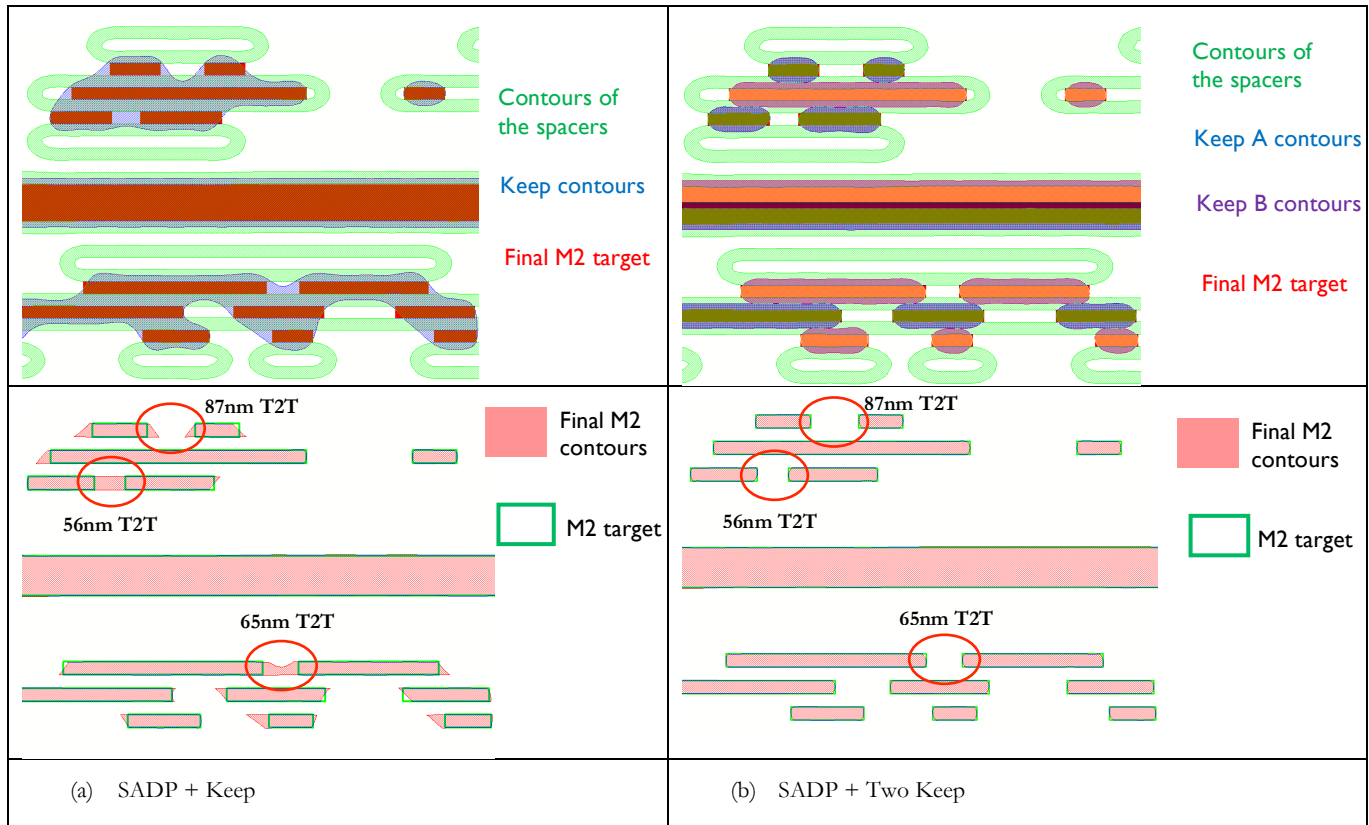


Figure 9: SADP + Keep vs. Two Keep simulation results

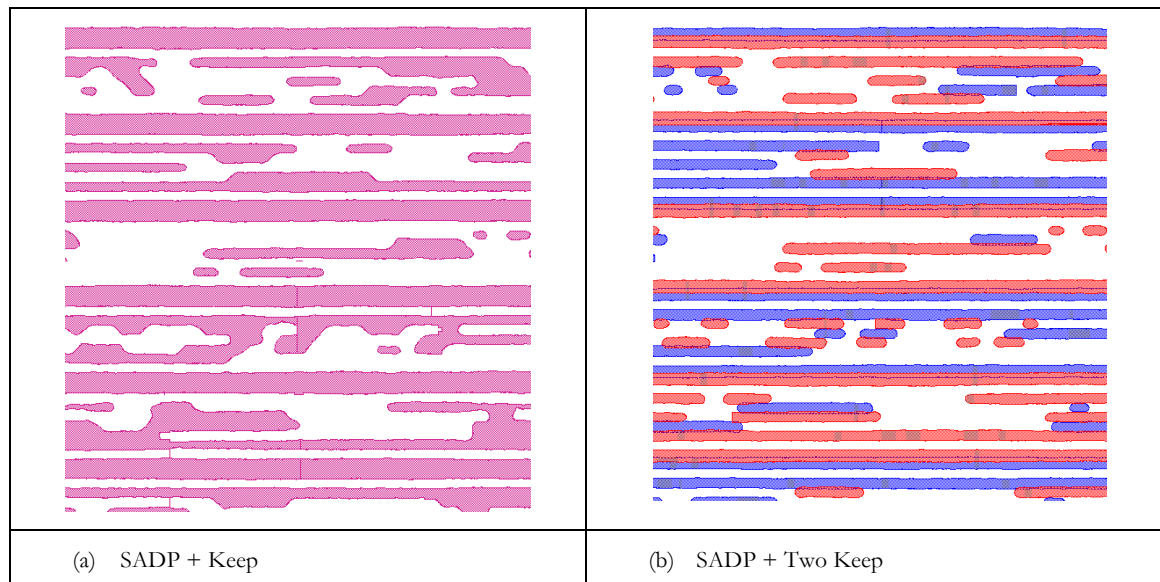


Figure 10: SADP+Keep vs. SADP+ Two Keep SEM extracted contours

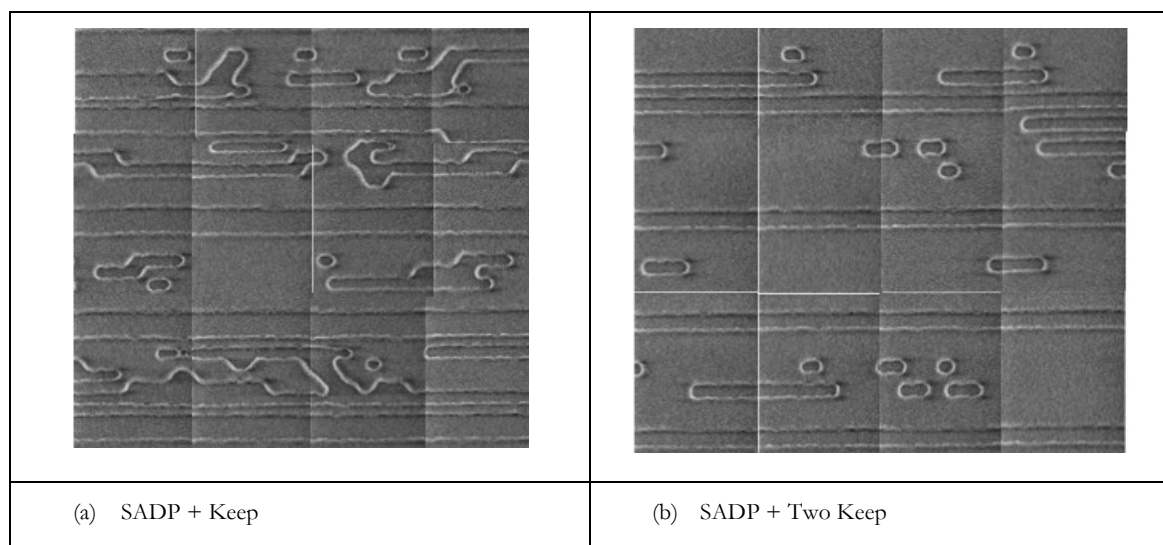


Figure 11: SADP+Keep vs. SADP+Two Keep SEM images

5. N7 Metal 32nm pitch: simulation results

A first consequence of the reduced metal pitch target of 28nm or 32nm for an N7 technology, there is a need to use an SAQP process instead of an SADP process. Assuming the mandrels are created well, our main problem is the block/keep layer once more. At these pitches a keep based strategy would not work. This would give raise to conflicts of coloring to allow good tip to tip printability and also odd cycles which may not allow 'colorability' in 3 colors or less for the keep masks.

Now going with the block strategy, we need to find the decomposition for the block mask. **Figure 12** shows a typical decomposed block layer for the line staggering approach. Whether a triple block is feasible or not depends on the exact metal pitch that is targeted. We believe that this approach could work for a 32nm pitch, but when moving to 28nm pitch a fourth color would be needed for the line stagger approach.

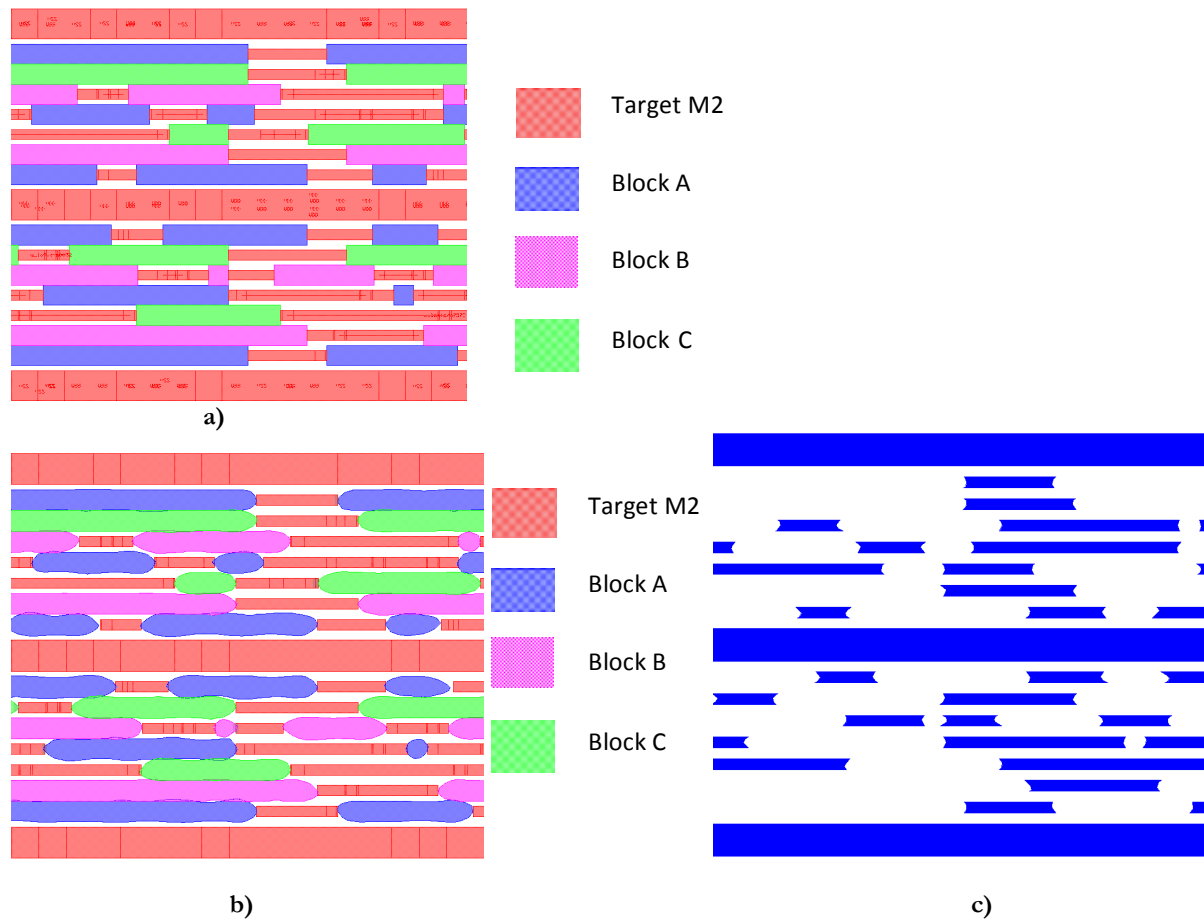


Figure 12: Staggered line approach a) Triple LE colored block layer, b) Simulated NC block, c) Simulated M2 nominal contours after full SADP + Block

Figure 13 shows the decomposition of the block masks and also computational litho simulation for the line cut approach of design where the line ends are aligned. For metal pitch 32nm, given that the line-cut approach can allow 2 colors for the block and is equal in process window with respect to line stagger, it is a superior approach even though it comes with the disadvantage of increased capacitance on the lines.

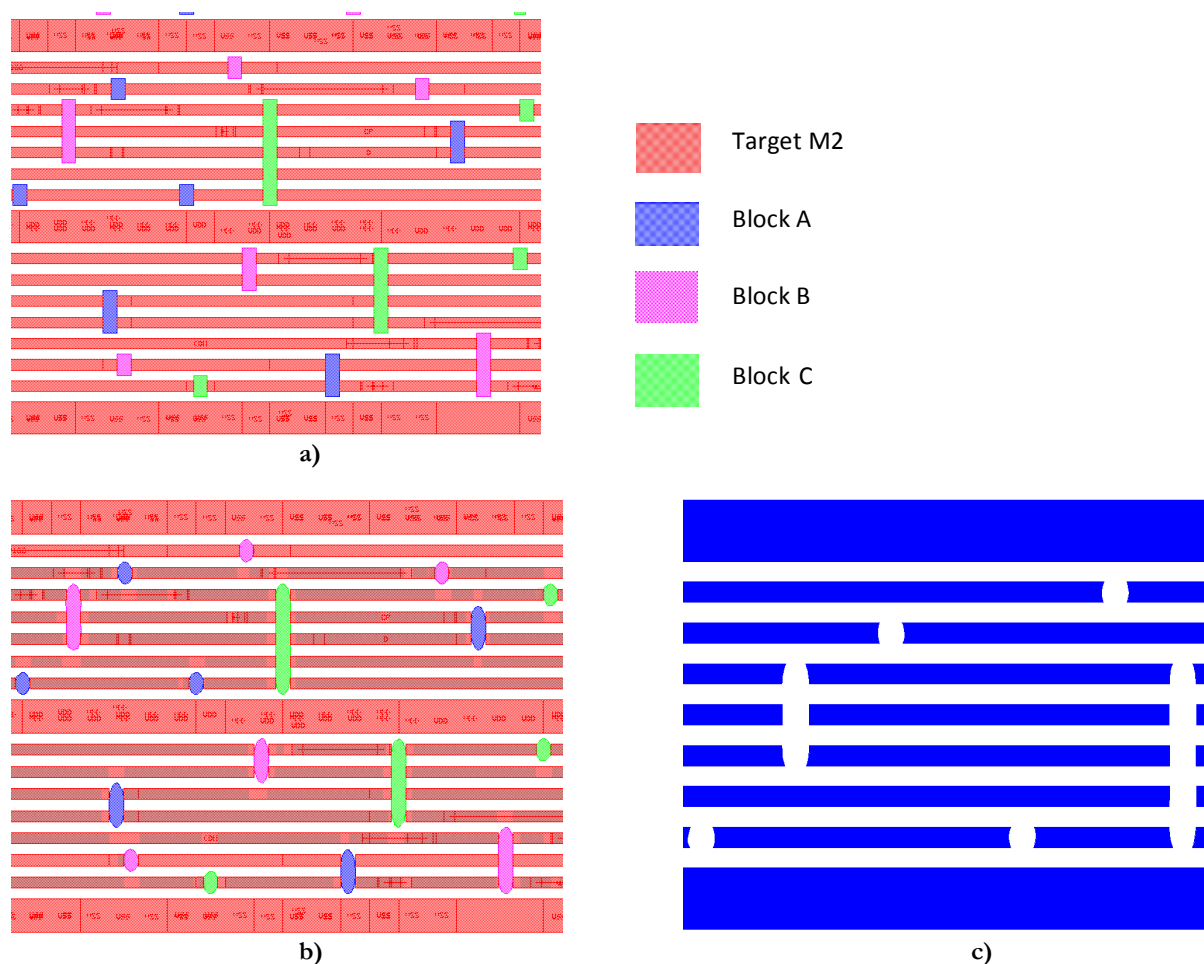


Figure 13: Line Cut approach a) LELELE colored block layer, b) Simulated NC Block, c) Simulated M2 nominal contours after full SADP + block

Conclusions

In this paper we discussed the different decomposition approaches and design approaches for tight pitch metal layers used for routing. From N10 metal pitches of 48nm down to N7 metal pitch down to 28nm we have done an analysis of the process window of different approaches. For N10, we showed on wafer that an SADP with two keep approach would allow to print in high fidelity giving the design freedom for all different constructs needed to reach high density logic place and route. We also showed the different decomposition approaches for tight pitch metals for an N7 technology. We showed that a block approach would work better than a keep approach. From design a line cut approach would be needed to allow lower number of colors needed for the block mask compared to the regular design style of ending metal where the via lands.

References

- [1] **Standard cell design in 7nm node: EUV versus immersion**, Bharani Chava, Peter Debacker, Yasser Sherazi, Praveen Raghavan, Werner Gillijns, David Rio, Ahmad Elsaid, Mircea Dusa, Julien Ryckaert, SPIE 2015
- [2] **DTCO at N7 and beyond: patterning and electrical compromises and opportunities** Diederik Verkest, Julien Ryckaert, Praveen Raghavan, Arindam Mallik, Sushil S. Sakhare, Bharani Chava, Yasser Sherazi, Philippe Leray, Abdelkarim Mercha, Jürgen Bömmels, Gregory R. McIntyre, Kurt G. Ronse, Aaron Thean, Zsolt Tökei, An Steegen, SPIE 2015